ABSTRACT OF THE DISCLOSURE

To perform gain adjustment of the amplitude of a binary phase shift keying (BPSK) wobble signal from a DVD to enable high-precision demodulation of address information, a peak detection circuit detects a peak value in a time period equal to or more than a half period of the input wobble signal. A gain computation circuit computes a gain adjustment coefficient from the peak value. The gain adjustment coefficient is limited to within a fixed range by a limiter and then supplied to a multiplier. To adjust digital-related delay generated when the gain adjustment coefficient is computed, the input wobble signal is delayed by a delay circuit before being supplied to the multiplier. The multiplier multiplies the wobble signal from the delay circuit by the gain adjustment coefficient and outputs the result as the digital AGC output.